IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:)
KUMAR ET AL.)
)
Serial No. **10/611,322**)
)
Confirmation No. **4030**)
)
Filing Date: **JULY 1, 2003**)
)
For: **DIGITAL ELECTRONIC CIRCUIT**)
FOR TRANSLATING HIGH VOLTAGE)
LEVELS TO LOW VOLTAGE LEVELS)
)

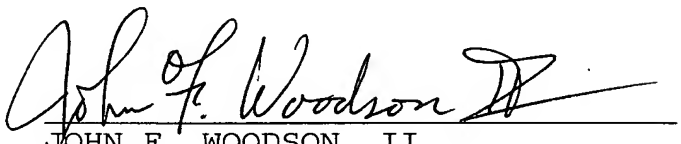
TRANSMITTAL OF CERTIFIED PRIORITY DOCUMENT

MS Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is a certified copy of the priority India Application No. 706/Del/2002.

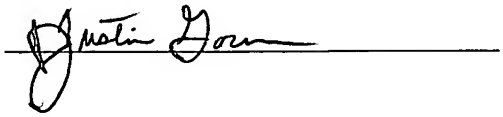
Respectfully submitted,



JOHN F. WOODSON, II
Reg. No. 45,236
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
Telephone: 407/841-2330
Fax: 407/841-2343
Attorney for Applicants

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: MS Missing Parts, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 29th day of October, 2003.



INTELLECTUAL PROPERTY **INDIA**

सत्यमेव जयते

GOVERNMENT OF INDIA
MINISTRY OF COMMERCE & INDUSTRY,
PATENT OFFICE, DELHI BRANCH,
W - 5, WEST PATEL NAGAR,
NEW DELHI - 110 008.

I, the undersigned, being an officer duly authorized in accordance with the provision of the Patent Act, 1970 hereby certify that annexed hereto is the true copy of the ***Application, Complete Specification*** *and* ***Drawing Sheets*** *filed in connection with Application for Patent No.* ***706/Del/02*** *dated* ***1sth July 2002.***

Witness my hand this 27th Day of June 2003.

(S.K. PANGASA)
Assistant Controller of Patents & Designs

Govt. of India Patent Office
New Delhi
Received Rs. ... Cash
on ...
Entry No. ... in the
Register of Valuables

0706 [redacted] 2

01 JUL 2002

FORM 1
THE PATENTS ACT, 1970
(39 of 1970)
APPLICATION FOR GRANT OF A PATENT
(See Sections 5(2), 7, 54 and 135)

1 I/we,

STMicroelectronics Pvt. Ltd., an Indian company, of Plot No. 2 & 3, Sector 16A, Institutional Area, Noida – 201 3001, Uttar Pradesh, India.

2 hereby declare –

(a) that I am/we re in possession of an invention titled "*Improved High To Low Voltage Level Translator For Digital Integrated Circuits.*"

(b) that the ~~provisional~~ / complete specification relating to this invention is filed with this application

(c) that there is no lawful ground of objection to the grant of a patent to me/us.

3 further declare that the inventor(s) for the said inventions is/are

(i) *KASANYAL Sunil Chandra, an Indian citizen, of Kasanyal Bhawan, Tildhukari, Pithoragarh, Uttaranchal, India.*

4 I/we claim the priority from the application(s) filed in convection countries, particulars of which are as follows: **NA**

5 I/we state that the said invention is an improvement in or modification of the invention the particulars of which are as follows and of which I/we are the applicant/patentee: **NIL**

6. I/we state that the application is divided out of my/our application, the particulars of which are given below and pray that this application be deemed to have been filed on under section 16 of the Act. **NIL**

7 That I am/we are the assignee or legal representative of the true and first inventors.

8 That my/our address for service in India is as follows:

ANAND & ANAND, Advocates
B-41, Nizamuddin East
New Delhi – 110 013

Tel Nos.: (11) 4355078, 4355076, 4350360
Fax Nos.: (11) 4354243, 4352060

ORIGINAL

9) Following declaration was given by the inventor(s) ~~or applicant(s) in the convention country~~:

I/we are the true and first inventors for this invention ~~or are~~ and the ~~applicant(s)~~ in the convention country declare that the applicant(s) herein is/are my/our assignee or legal representative

KASANYAL Sunil Chandra

Date: 1st July, 2002

10) that to the best of my/our knowledge, information and belief the fact and matters stated herein are correct and that there is no lawful ground of objection to the grant of patent to me/us on this application.

11) Followings are the attachment with the application:

(a) ~~provisional/~~ complete specification (3 copies)

(b) Form 1 (in triplicate)

(c) Formal Drawings (3 copies)

(d) Statement and Undertaking on Form 3

(e) Fee Rs. 5000.00 In cash/cheque/bank draft bearing no. , dated 1st July, 2002 on Citibank Bank.

I/we request that a patent may be granted to me/us for the said invention.

Dated this 1st day of July, 2002

of Anand And Anand Advocates
Attorney for the Applicant

To
The Controller of Patents
The Patent Office, Delhi

01 IND-316

Form 2

THE PATENTS ACT, 1970

COMPLETE SPECIFICATION

01 JUL 2002

[See Section 10]

"IMPROVED HIGH TO LOW VOLTAGE LEVEL TRANSLATOR FOR DIGITAL INTEGRATED CIRCUITS"

ORIGINAL

STMicroelectronics Pvt. Ltd., *Plot No. 2 & 3, Sector 16A, Institutional Area, Noida – 201 301, Uttar Pradesh, India, an Indian Company*

The following specification particularly describes and ascertains the nature of this invention and the manner in which it is to be performed.

IMPROVED HIGH TO LOW VOLTAGE LEVEL TRANSLATOR FOR DIGITAL INTEGRATED CIRCUITS

Field of the Invention :

This invention relates to an improved voltage level translator for translating high to low voltage levels in digital intergrated circuits. This invention further relates to an improved method for translating high voltage levels in digital intergrated circuits.

Background of the invnetion:

Advances in semiconductor fabrication and manufacturing techniques have led to smaller, denser and more complex integrated circuits. Digital integrated circuits are spearheading the drive to increased densities and smaller geometries. At the same time digital integrated circuits are also being operated at higher speeds. The combination of increased density and higher speeds has a tendency to increase power dissipation.which in turn results in increased temperature of the device which reduces device reliability. To counteract the increased power dissipation modern devices are increasingly being designed to operate at reduced voltage levels. Current technology supports digital integrated circuits based on transistors with gate lengths reduced to 0.12u with corresponding supply voltages as low as 1.2V. However the IO requirements of digital integrated circuits are defined by the requirements of external devices and hence remain at voltage levels that are not significantly higher than the core circuitry. Typical IO voltages remain at a 3.3v to 5.0V level while the core circuitry operates at 1.2V. To operate in such an environment it is necessary to use voltage level translators, which translate signals at the higher voltage level of IOs to the lower voltage levels of the core logic.

A transistor operating at a higher voltage such as 3.3V is designed to have a relatively long gate length to avoid punchthrough. At the same time the transistor must also have a thicker gate oxide thickness to prevent oxide break down. These transistors are relatively high voltage devices and are termed as 3.3V devices in the present invention. If a 3.3V device is used for operation at lower voltage levels such as 1.2V, it provides relatively poor performance in term of speed owing to higher channel resistance and higher gate capacitance. In contrast, transistors operating at lower voltage levels are designed with

shorter channel lengths to reduce the channel resistance and gate capacitance as the breakdown voltage requirements are lower. The lower resistance and gate capacitance enables significant increase in speed of operation besides providing higher density. Transistors which are used for lower voltages are low voltage devices and if designed for 1.2V operation are termed as 1.2V devices in this document. Low voltage transistor models are not designed for use with higher voltages because of the risk of punchthrough and gate oxide breakdown.

Fig.1. shows a conventional high to low voltage translator using two cascaded CMOS inverters **30** and **40**. The first inverter operates at the higher supply voltage **VCC1**, while the second inverter operates at the lower voltage **VCC2**. Since the first inverter 30 is required to handle a higher voltage level signal swing (**VCC1**) at its input **20** and to operate using a higher power supply voltage **VCC1** it is constructed using higher voltage transistors. Accordingly NMOS transistor **21** and PMOS transistor **22** are VCC1 level transistors. The output of the first inverter at node **23** which is the input to the second inverter has a swing of **VCC1** hence the second inverter **40** operating from the lower power supply voltage **VCC2** is also required to use higher voltage devices (**VCC1** level devices) similar to those used in the first inverter **30**, inorder to avoid oxide breakdown of transistors NMOS transistor **27** and PMOS transistor 26. If the voltage translation is from 3.3V to 2.5V it is possible to use 2.5V transistors as the tolerance limits of these devices extend upto 3.3V. However if the 2 supply voltages are 3.3V and 1.2V then the transistors of second inverter **40** must be 3.3V devices, having the higher gate length and thicker gate oxide required for 3.3V signals. This results in poor performance relative to the rated performance of 1.2V devices.

The primary factor in performance degradation relates to the rising edge of the input signal. When the input signal is at a high level the input to the second inverter **40** is 0V, accordingly the gate-to-Source Vgs for its PMOS transistor **26** is -1.2V.Since the PMOS transistor **26** is designed to give good performance for Vgs=- 3.3V it exhibits poor performance for Vgs=-1.2V. At the same time, inorder to drive the external load at the output of the translator, the size of the PMOS transistor **26** operating at the sub-optimal Vgs needs to be increased significantly, thereby increasing gate capacitance and worsening performance (significantly increased rise time), and enhanced power dissipation. In addition, the propagation delay is

also increased together with increased difference between rise time and fall time which degrades the performance of subsequent stages of the integrated circuit. Finally, the increased gate to drain capacitance of the PMOS transistor of the second inverter increases the bootstraping effect further increasing propagation delay and output transition time.

SUMMARY OF THE INVENTION

The object of this invention is to obviate the above drawbacks and provide a high- to low-voltage translator offering reduced rise-times.

Another object of this invention is to provide a high- to low- voltage translator offering equal rise- and fall- times and equal transition times.

Yet another object of the invention is to provide a high- to low- voltage translator with reduced propagation delay.

Finally, another object of the invention is to provide a high- to low- voltage translator with reduced power dissipation.

To achieve these and other objects the invention provides an improved high to low voltage translator for digital integrated circuits comprising a digital inverter operating at the higher voltage level having its output connected to a voltage limiting circuit that limits the voltage applied at the input of a second digital inverter operating at the lower voltage level, and providing the final output of the voltage level translator. The voltage limiting circuit comprises an inverter operating from the higher voltage supply driving the control terminal of a low-voltage transistor having its common terminal connected to the low-voltage supply while its output terminal is connected to the output terminal of a transistor having its control terminal connected to the input of the voltage limiting circuit, while its common terminal provides the complementary output from the voltage limiting circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects and advantages of the invention will become more apparent in reference to the following description and the accompanying drawings, wherein:

FIG.1 shows the convetional method for translating high voltage levels into low voltage levels.

FIG.2 shows the scheme for translating high voltage levels into low voltage levels according to the invention.

FIG.3 shows the preferred embodiment of the circuit for voltage translation.

FIG.4 shows a preferred embodiment of the complete voltage translator with output signal having same polarity as the input signal.

FIG.5 shows another preferred embodiment of the circuit of the voltage translator.

DETAILED DESCRIPTION OF THE INVENTION

Fig.-1 has already been described in the background to the invention.

FIG.2 shows a voltage translator for translating higher voltage levels into lower voltage levels according to this invention. Signal IN at terminal **51** has swing from 0 V to a high voltage level of VCC1 (say **3.3V**). Terminal **51** is directly connected to the gate **53** of NMOS transistor **55**. The source of NMOS transistor **55** is connected to ground GND and the drain is connected to terminal **57** named OUT. Terminal **57** is the low voltage output of the circuit for loads operating at the lower voltage VCC2 (say **1.2V**) providing a voltage swing at **57** from **0V** to **1.2V**. Since the NMOS transistor **55** has an input swing of **3.3V** it must use **3.3V** device NMOS transistors having a higher gate length and thicker gate oxide compatible to 3.3V operation. Transistor **55** gives good performance for Vgs=3.3V. When the signal at **51** is at logic'0' it provides a voltage of 0V which turns off transistor **55**. When the signal at **51** is at Logic'1' it provides a voltage of 3.3V at the gate **53** of transistor **55**, which turns it on. When transistor **55** is on, its Vgs=3.3V which enables good sinking capability providing a rapid falling edge of the signal at **57**. PMOS transistor **54** has its drain connected to **57**, while its source is connected to power supply VCC2 which is 1.2V. Its gate is coupled to terminal

52 which is the output of **Logic Block 100**. Since the source voltage of **PMOS** transistor **54** is only at 1.2V, **PMOS** transistor **54** should be a 1.2V device in order to get good rise-time performance. For this it would have a shorter gate length and thinner gate oxide as compared to that of 3.3V rating transistors. Also the voltage swing at the gate of **54** should be limited to 1.2V to prevent oxide break down.

Logic circuit 100 which is connected between terminal **51** and **52**, provides these facilities by taking the input from **51** with a voltage swing of 0V to 3.3V and providing output at terminal **52** with a voltage swing of 0V to 1.2V. The output of **Logic Block 100** is non-inverting. A 0V input generates a 0V output while a 3.3V at **51** generates a 1.2V output at **52**. The functioning of **Logic Block 100** is such that it allows a 0V input to pass through it but when the signal at **51** rises above 0V the output **52** follows it until it reaches 1.2V after which the voltage level saturates. **Logic Block 100** maintains the output **52** at 1.2V until the signal at **51** starts decreasing from 3.3V and reaches 1.2V after which the output **52** again follows **51** down to 0V. In this manner the voltage swing of 0V to 3.3V at **51** is translated to 0V to 1.2V swing at **52** by **Logic Block 100**.

FIG.3 shows a preferred embodiment of **Logic Block 100**. The Logic Block is essentially an inverter **200** having an **NMOS** transistor **202** and a **PMOS** transistor **201**. The gate of **NMOS** transistor **202** is connected to input terminal **51**, its drain is connected to the net **204** and its source is connected to ground. The gate of **PMOS** transistor **201** is also connected to input terminal **51** while its drain is connected to the net **204** and its source is connected to the higher supply voltage **VCC1.** Since this inverter **200** experiences an input swing from 0V to **VCC1** and operates from the higher power supply **VCC1** it uses higher voltage devices for **NMOS** transistor **202** and **PMOS** transistor **201**. The gate of **NMOS** transistor **102** is connected to the net **204**, while its drain is connected to net **52** and its source is connected to input terminal **51**. Since the swing at the source and gate of **NMOS** transistor **102** is from 0 to the higher voltage level **VCC1** it must be a high voltage device. The gate of **PMOS** transistor **103** is connected to the net **204**, while its drain is connected to net **52** and its source is connected to the lower voltage level **VCC2**. Since the voltage swing at the gate of transistor **103** is from 0 to the higher voltage level VCC1 it must be a high voltage device.

When the signal at input terminal 51 is at 0V, the gate of NMOS transistor 55 is at 0V, causing it to turn off. This produces a VCC1 level at the net 204 of the inverter 200. VCC1 at 204 turns NMOS transistor 102 on and turns off PMOS transistor 103. Since NMOS transistor 102 is on, it passes the 0V from input terminal 51 to its output 52, causing PMOS transistor 54 to turn on. This provides a signal of VCC2 at net 57. When the signal at input terminal 51 starts increasing from 0V, the gate voltage of NMOS transistor 55 follows terminal 51. The width of transistors 201 and 202 are selected to adjust the trip point of inverter 200 to a level equal to VCC2, Therefore as the signal at net 51 reaches VCC2 it trips inverter 200 causing 0V to appear at the net 204. The 0V at output 204 turns-off NMOS transistor 102 and isolates the net 52 from net 51. This stops further propagation of the signal from terminal 51 to net 52. Also the 0V at net 204 turns on PMOS transistor 103 thereby connecting net 52 to the VCC2 supply voltage. The VCC2 voltage at net 52 turns off PMOS transistor 54. When the voltage at terminal 51 increases from 0V and reaches a value equal to the threshold voltage of NMOS transistor 55 it turns on the transistor and applies 0V at terminal 57. In this manner the input swing of 0V to VCC1 at terminal 51 is converted to a voltage swing of 0V to VCC2 at terminal 57, but with a polarity opposite to the polarity of the input of the circuit. Since the load for Logic Block 100 is limited to the small gate capacitance of PMOS transistor 54, the required size for NMOS transistor 102 is small and also the slew rate at net 52 is approximately the same as at net 51.

FIG.4 shows a voltage translator with output signal having same polarity as that of input signal. For acheiving the same polarity an inverter 300 is connected at the output terminal 57 of the ciruit of FIG.3. PMOS transistor 301 of inverter 300 has its gate connected to the net 57, its drain connected to terminal 58 and its source connected to the VCC2 supply. Since input swing for PMOS transistor 301 is 0 to VCC1, and its supply voltage is VCC2, it should be a VCC2 device. NMOS transistor 302 of inverter 300 has its gate connected to net 57, its drain is connected to terminal 58 and its source is connected to ground. The input swing for NMOS transistor 302 is from 0V to VCC2 and the voltage which appears at its input is VCC2, it should be a VCC2 device. The sizes of PMOS transistor 301 and NMOS transistor 302 are adjusted according to the load at terminal 58, to get the required slew rates at terminal 58 and to get better delays. In this manner the required driving capability is achieved by incresing the driving capability of inverter 300. In addition, by sizing the width

of NMOS transistor **302** and PMOS transistor **301**, the rise delays and fall delays can be made equal and the slew rates can be adjusted according to requirements. Since its load is limited to inverter **300** the size of PMOS transistor **54** can be as low as 1/2.5 times the size of inverter **300.** This reduces the loading for the signal at **51** and for NMOS transistor **102** and therby reduces the propagation delay.

FIG.5 shows a preferred embodiment of circuitry for a complete voltage translator with the output signal at terminal **57** having the same polarity as the input signal at terminal **60.** In this circuit an inverter **400** is connected before the terminal **51** of **FIG.3**. **PMOS** transistor **401** of inverter **400** has its gate connected to the input terminal **60,** while its drain is connected to net **51** and its source is connected to the VCC1 power supply. **NMOS** transistor **402** has its gate connected to the input terminal **60**, while its drain is connected to net **51** and its source is connected to ground. Since both the **NMOS** and **PMOS** transistors have an input signal swing of VCC1 at their gates and operate off a VCC1 power supply, both are required to be VCC1 devices.

It will be apparent to those with ordinary skill in the art that the foregoing is merely illustrative and is not intended to be exhaustive or limiting, having been presented by way of example only and that various modifications can be made within the scope of the above invention. For example, the voltage limiting circuit may provide an inverting output instead of a non-inverting output.

Accordingly, this invention is not to be considered limited to the specific examples chosen for purposes of disclosure, but rather to cover all changes and modifications, which do not constitute departures from the permissible scope of the present invention. The invention is therefore not limited by the description contained herein or by the drawings, but only by the claims.

We claim:

1. An improved high to low voltage translator for digital integrated circuits, comprising :
   - a first digital inverter operating at the higher voltage level, and having its input connected to the input of the voltage translation circuit and its output connected to,
   - a voltage limiting circuit that limits the voltage applied at the input of,
   - a second digital inverter operating at the lower voltage level, and providing the final output of the voltage level translator.

2. An improved high to low voltage translator for digital integrated circuits as claimed in claim 1, wherein the voltage limiting circuit comprises :
   - an inverter operating from the higher voltage supply and having its output connected to,
   - the control terminal of a low-voltage transistor having its common terminal connected to the low-voltage supply while its output terminal is connected to,
   - the output terminal of a transistor having its control terminal connected to the input of the voltage limiting circuit, while its common terminal provides the complementary output from the voltage limiting cirucit.

3. An improved method for providing high to low voltage translation comprising the steps of :
   - limiting the output from the high-voltage digital inverter to the desired lower voltage levels, and
   - using the limited voltage swing to drive an output low-voltage digital inverter.

4. An improved method for providing high to low voltage translation as claimed in claim 3, wherein the output from the high-voltage digital inverter is converted to the desired low voltage levels by voltage limiting it to the levels of the low voltage supply.

5. An improved high to low voltage translator for digital integrated circuits substantially as herein described with reference to and as illustrated in figures 2 to 5 of the accompanying drawings.

6. An improved method for providing high to low voltage translation substantially as herein described with reference to and as illustrated in figures 2 to 5 of the accompanying drawings.

Dated this 1st day of ~~June~~ July 2002

of **ANAND & ANAND, Advocates**
Agents for the Applicants

ABSTRACT

The present invention provides an improved high to low voltage translator for digital integrated circuits comprising a digital inverter operating at the higher voltage level having its output connected to a voltage limiting circuit that limits the voltage applied at the input of a second digital inverter operating at the lower voltage level, and providing the final output of the voltage level translator. The voltage limiting circuit comprises an inverter operating from the higher voltage supply driving the control terminal of a low-voltage transistor having its common terminal connected to the low-voltage supply while its output terminal is connected to the output terminal of a transistor having its control terminal connected to the input of the voltage limiting circuit, while its common terminal provides the complementary output from the voltage limiting circuit.

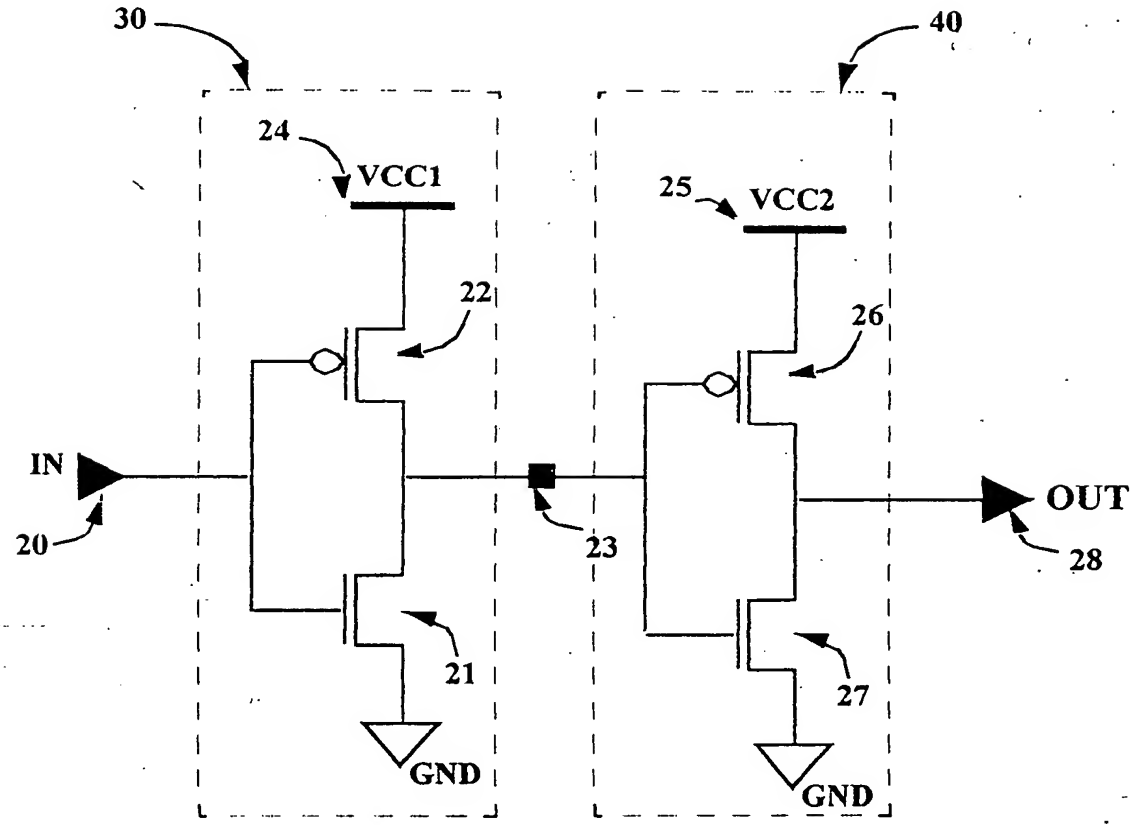


FIG.1 CONVENTIONAL METHOD

of **ANAND & ANAND, Advocates**
Agents for the Applicants

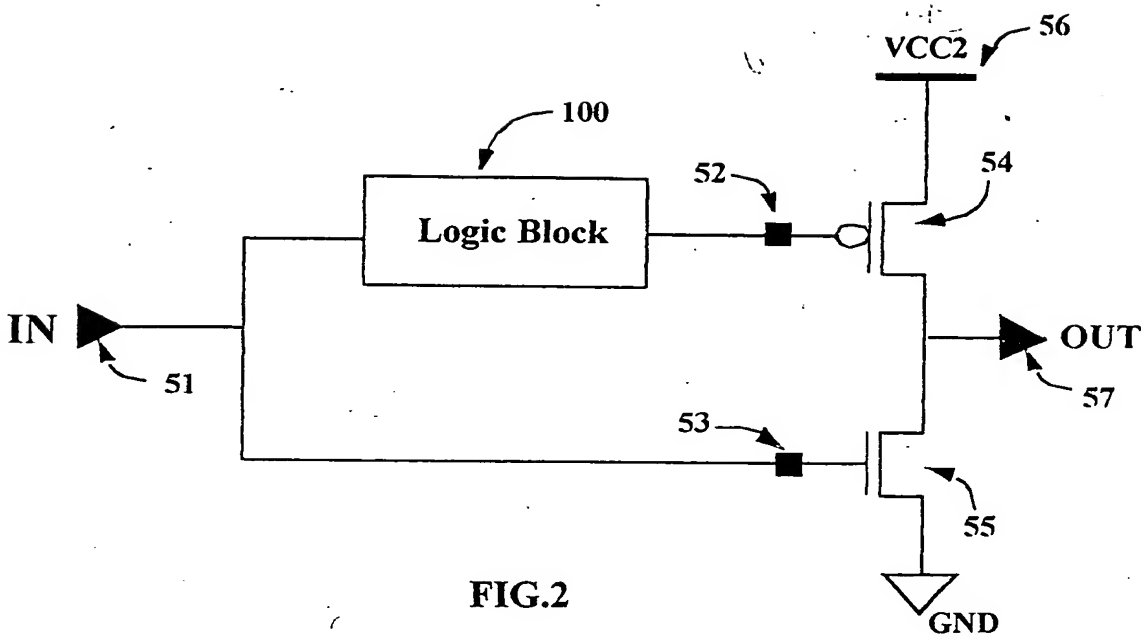


FIG.2

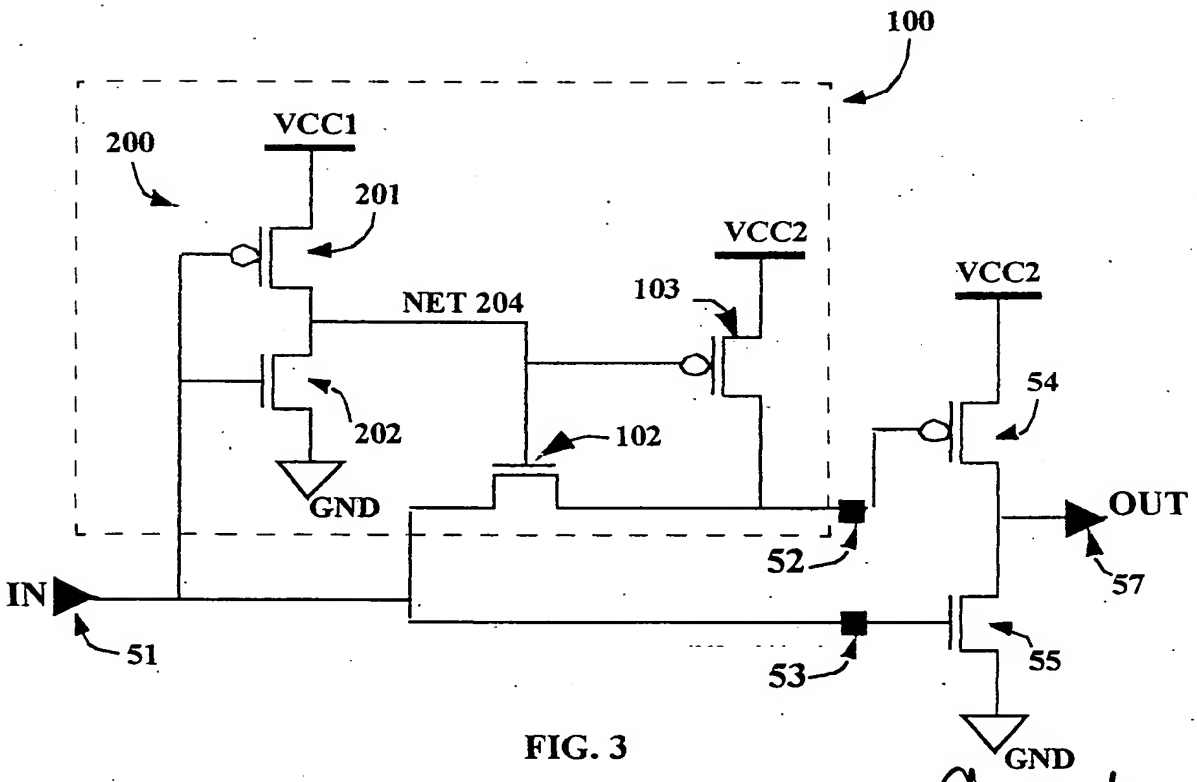


FIG. 3

of ANAND & ANAND, Advocates
Agents for the Applicants

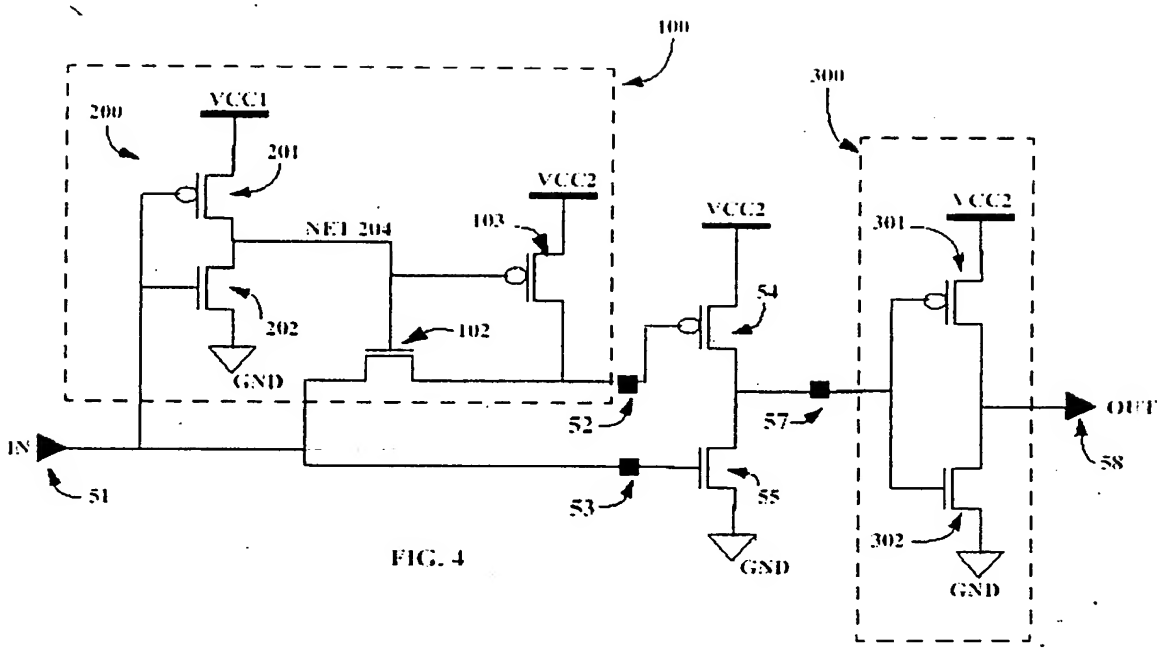


FIG. 4

of **ANAND & ANAND, Advocates**
Agents for the Applicants

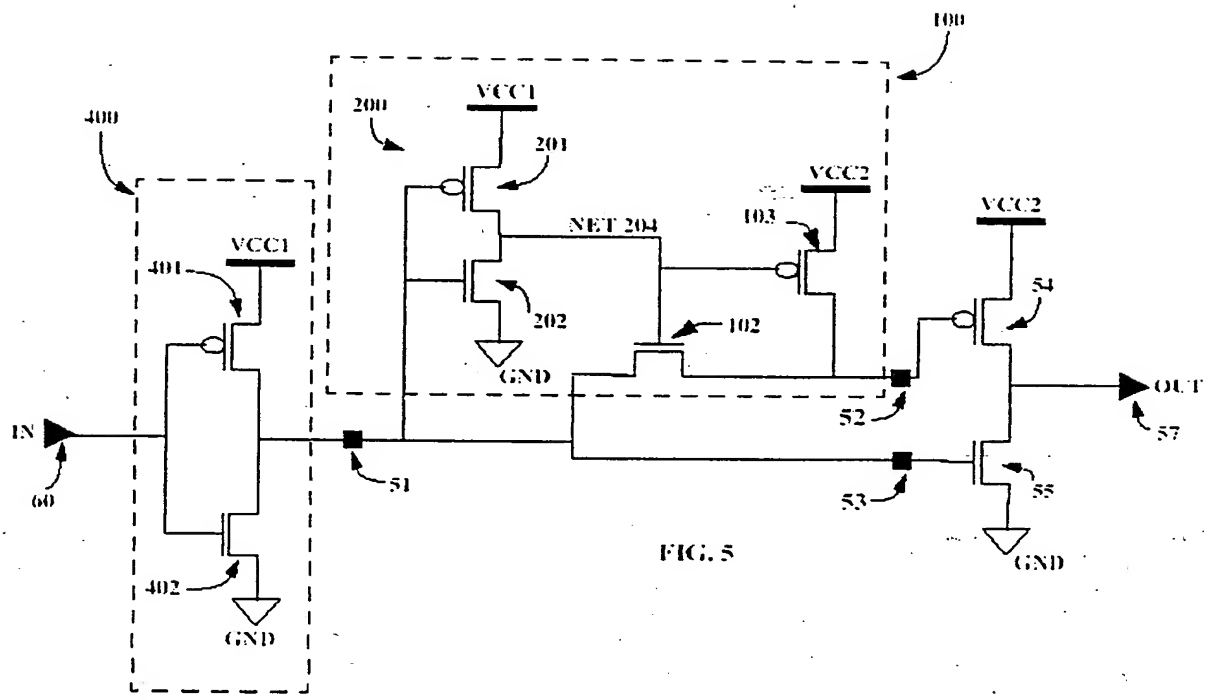


FIG. 5

of **ANAND & ANAND, Advocates**
Agents for the Applicants